WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a silicon substrate having a major surface;

a plurality of silicon columns formed on the major surface of the silicon substrate;

a plurality of transistors formed on the side surface of the respective silicon columns, each of the transistors comprising

a first impurity layer formed on an upper surface of corresponding one of the silicon columns and serving as one of a source and a drain;

a second impurity layer formed on a bottom of a trench adjacent to the corresponding one of the silicon columns and serving as the other of the source and the drain and, together with the second impurity layer of the rest of the transistors, connected to a constant voltage terminal;

a channel portion formed on a side surface of the corresponding one of the silicon columns between the first impurity layer and the second impurity layer;

a gate insulating film formed on the channel portion; and

a gate electrode formed over the channel portion with the gate insulating film interposed therebetween; and

a plurality of capacitors each having two electrodes, one of the two electrodes being connected

to the first impurity layer.

2. The semiconductor memory device according to claim 1, wherein the plurality of capacitors are formed on the plurality of silicon columns, each of the capacitors being a stacking type capacitor having a capacitor electrode connected to the first impurity layer and being the one electrode, a dielectric film formed on the capacitor electrode, and a storage electrode opposing the capacitor electrode through the dielectric film.

3. The semiconductor memory device according to claim 2, wherein the stacking type capacitor has a planar size substantially same as that of the upper surface of the respective silicon columns.

4. The semiconductor memory device according to claim 1, further comprising a connection line configured to bringe the second impurity layer out to the major surface of the semiconductor substrate.

5. A semiconductor memory device comprising:

a silicon substrate of a first conductivity type having a grid-like trench extending in an x direction and a y direction substantially orthogonal to the x direction on a major surface thereof, the trench having a width A;

a plurality of silicon columns formed on the major surface of the substrate and having a square upper surface defined by the trench, the square upper surface

having a side length B;

a plurality of the transistors each formed on a side surface of the respective silicon columns, each of the transistors comprising

a first impurity layer formed on the square upper surface of corresponding one of the silicon columns and serving as one of a source and a drain;

a second impurity layer formed on a bottom of the trench adjacent to the corresponding one of the silicon columns and serving as the other of the source and the drain;

a channel portion formed on a side surface of the corresponding one of the silicon columns between the first impurity layer and the second impurity layer;

a gate insulating film formed on the channel portion; and

a gate electrode formed over the channel portion with the gate insulating film interposed therebetween; and

a plurality of capacitors each having two electrode, one of the two electrodes being connected to the first impurity layer.

6. The semiconductor memory device according to claim 5, wherein the width A of the trench is equal to the side length B of the upper surface of the respective silicon columns.

7. The semiconductor memory cell according to claim 5, wherein the plurality of capacitors are formed on the plurality of silicon columns, respectively, each of the capacitors comprising

a capacitor electrode connected to the first impurity layer and being the one electrode;

a dielectric film formed on the capacitor electrode; and

a storage electrode opposing the capacitor electrode through the dielectric film.

8. The semiconductor memory device according to claim 7, wherein the stacking type capacitor has a planar size substantially same as the upper surface size of the silicon column.

9. The semiconductor memory device according to claim 5, further comprising a connection line configured to bring the second impurity layer, which is connected to the second impurity layer of an adjacent one of the transistors, out to the major surface of the silicon substrate.

10. The semiconductor memory device according to claim 9, further comprising a bit line formed above the major surface of the silicon substrate,

wherein the connection line is insulatively buried in the trench so as to extend from the second impurity layer on the bottom of the trench to an upper side of the trench and be connected to the bit line.

11. The semiconductor memory device according to claim 10, wherein the gate electrode is so formed as to surround the corresponding one of the silicon columns and, when the gate electrodes of the silicon columns aligned in one direction are continuously connected to form a word line, the connection line is formed in the trench at a central area surrounded by mutually adjacent four of the silicon columns.

12. The semiconductor memory device according to claim 10, wherein the gate electrode is formed on one side surface of the corresponding one of the silicon columns and, when the gate electrodes of the silicon columns aligned in one direction are continuously connected to form a word line, the connection line is formed in the trench along another side surface adjacent to the one side surface of the corresponding one of the silicon columns.

13. The semiconductor memory device according to claim 10, wherein an aligning pitch of the silicon columns in an extending direction of the bit line is made loose at a site where the second impurity layer is connected to the connection line at the bottom of the trench.

14. The semiconductor memory device according to claim 5, wherein the second impurity layer is formed as a band-like configuration around the corresponding one of the silicon columns.

15. The semiconductor memory device according to claim 5, wherein the second impurity layer is united with respect to adjacent three or more of the silicon columns on the bottom of the trench.

16. The semiconductor memory device according to claim 5, wherein the plurality of silicon columns form an array of a matrix form and one pair of the silicon columns at both corners on a diagonal line of the matrix form are lacking.

17. A method for manufacturing a semiconductor memory device comprising:

forming a plurality of silicon columns on a major surface of a semiconductor substrate of a first conductivity type, using a mask to form the plurality of silicon columns, each of the silicon columns having a square configuration of one side length B, which is defined by a grid-like trench extending in an x direction and in a y direction substantially orthogonal to the x direction, the trench having a width A;

forming a plurality of impurity layers of a second conductivity type on a bottom of the trench and on a top surface of the silicon columns, respectively;

forming a gate electrode on each side surface of the silicon columns which faces the trench formed in an x direction through a gate insulating film; and

forming a capacitor having a square planar configuration of one side length B and aligned with the

top surface of the respective silicon columns in the x direction and at least containing a portion formed just on the top surface of the silicon column in the y direction.

18. The method according to claim 17, wherein the forming of a plurality of the silicon columns includes forming the silicon columns with use of the mask which is set at B=A.

19. The method according to claim 17, wherein the forming of a plurality of silicon columns includes

performing a first light exposure with use of the mask which is set at B=A/3, and

performing a second light exposure by shifting the mask by $2^{1.5}B$ in a direction substantially 45° to the x direction or the y direction.

20. The method according to claim 19, wherein the forming of a capacitor includes

performing a first light exposure with use of the mask for capacitors each having a square configuration of one side length B=A/3, and

performing a second light exposure by shifting the mask by $2^{1.5}B$ in a direction substantially 45° to the x direction or y direction.

21. The method according to claim 17, further comprising forming a connection line connected to the impurity layer at the bottom of the trench and brought out to the main surface of the semiconductor substrate.